REMARKS

In the Official Action mailed on **March 12, 2004,** the Examiner reviewed claims 1-20. Claims 1-20 were rejected were rejected under 35 U.S.C. §103(a) as being unpatentable over Chaudhry et al. (USPub 2002/0157056, hereinafter "Chaudhry") in view of Arimilli et al., (USPN 6,480,975, hereinafter "Arimilli").

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 10, and 19 were rejected as being unpatentable over Chaudhry in view of Arimilli. Applicant respectfully points out that Arimilli teaches an error correcting mechanism coupled to a cache to **correct errors within the cache** (see Arimilli, col. 2, lines 10-17 and col. 4, lines 32-52).

In contrast, the present invention is directed to determining that a data item is in a cache while the memory controller sweeps the main memory for errors and if so, retrieving the data from the cache, correcting any errors, and **returning the data to memory** (see page 9, line 24 to page 10, line 6 of the instant application). Determining that a data item is in a cache while the memory controller sweeps the main memory for errors, retrieving the data from the cache, correcting any errors, and returning the data to memory is beneficial because it ensures that data in the main memory is correct even when the data has been checked out to cache. Note that unlike the combined system of Chaudhry and Arimilli, the present invention does not require the cache to store error correcting codes with cachelines; it only requires error correcting codes in main memory. Note also that it is difficult to support error correcting codes in cache for the reasons discussed in Chaudhry (see Chaudhry, paragraph [0010]). Further note that the present invention corrects errors in main memory and in the cache using the same mechanism located in the memory controller instead of using separate mechanisms. Note that it greatly complicates cache design to incorporate error correcting codes into the cache.

There is nothing within Chaudhry or Arimilli, either separately or in concert, which suggests determining that a data item is in a cache while the memory controller sweeps the main memory for errors, retrieving the data from the cache, correcting any errors, and returning the data to memory.

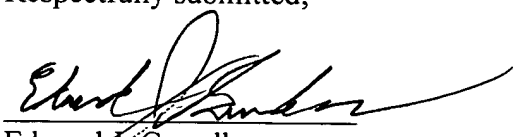
Accordingly, Applicant has amended independent claims 1, 10, and 19 to clarify that the present invention determines that a data item is in a cache while the memory controller sweeps the main memory for errors, retrieves the data from the cache, corrects any errors, and returns the data to memory. These amendments find support on page 9, line 24 to page 10, line 6 of the instant application.

Hence, Applicant respectfully submits that independent claims 1, 10, and 19 as presently amended are in condition for allowance. Applicant also submits that claims 2-9, which depend upon claim 1, claims 11-18, which depend upon claim 10, and claim 20, which depends upon claim 19 are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

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